WHAT IS CLAIMED IS:

1. A random access memory, comprising:

a latching circuit configured to receive a first signal and provide a second signal corresponding to the first signal to latch data signals into the random access memory; and

a logic circuit configured to provide a first response after a predetermined number of the data signals have been latched into the random access memory by the second signal, wherein the latching circuit is configured to receive the first response and lock the second signal to a logic level based on the first signal and the first response to prevent inadvertent latching of other data signals.

2. The random access memory of claim 1, wherein the latching circuit comprises:

a first latch electrically coupled to the logic circuit; and

a second latch electrically coupled to the first latch.

3. The random access memory of claim 1, wherein the latching circuit comprises:

a first latch configured to receive the first response and provide a second response based on the first response and the first signal; and

a second latch configured to receive the second response and lock the second signal to the logic level based on the first signal and the second response.

4. The random access memory of claim 1, wherein the logic circuit comprises a counter configured to count clock cycles that correspond to the data signals latched into the random access memory.

5. The random access memory of claim 1, wherein the logic circuit comprises a shift register configured to shift in response to clock cycles that correspond to the data signals latched into the random access memory.

6. The random access memory of claim 1, wherein the logic circuit is configured to respond to positive edges of a clock signal after a write command to determine the predetermined number of the data signals latched into the random access memory.

7. The random access memory of claim 1, wherein the logic circuit comprises a counter configured to be reset by a write command signal.

8. The random access memory of claim 1, wherein the logic circuit comprises a shift register configured to be reset by a write command signal.

9. The random access memory of claim 1, wherein the logic circuit is configured to receive a write command signal that resets the logic circuit.

10. The random access memory of claim 1, wherein the logic circuit is configured to receive burst length infomation that sets the predetermined number of the data signals to a burst length value.

11. The random access memory of claim 1, wherein the logic level is a low logic level.

12. A random access memory, comprising:

a logic circuit configured to receive a clock signal and provide a first response after a predetermined number of clock edges have been received from the clock signal;

a first latch circuit configured to receive the first response and a first signal and provide a second response based on the first response and the first signal; and

a second latch circuit configured to receive the second response and the first signal and provide a corresponding second signal, wherein the second latch circuit is configured to lock the second signal to a logic level based on the second response and the first signal.

13. The random access memory of claim 12, wherein the logic circuit comprises a counter configured to receive burst length information that comprises the predetermined number of clock edges and receive a write command signal that is an indication to start counting the clock edges.

14. The random access memory of claim 12, wherein the logic circuit comprises a shift register configured to receive burst length information that comprises the predetermined number of clock edges and receive a write command signal that is an indication to start shifting the shift register in response to the clock edges.

15. The random access memory of claim 12, wherein the random access memory is a double data rate synchronous dynamic random access memory.

16. The random access memory of claim 12, wherein the random access memory is a DDR-I SDRAM.

17. The random access memory of claim 12, wherein the random access memory is a DDR-II SDRAM.

18. A random access memory comprising:

a locking circuit that receives a first data strobe and generates a second data strobe from the first data strobe, wherein the second data strobe latches input data during a write operation and is locked at a logic level after the input data is latched.

19. The random access memory of claim 18, wherein the locking circuit comprises a counter configured to start counting in response to a write command signal and count bursts of input data up to a burst length to determine that the input data is latched.

20. The random access memory of claim 18, wherein the locking circuit comprises a shift register configured to start shifting in response to a write command signal and shift up to a burst length to determine that the input data is latched.

21. The random access memory of claim 18, wherein the memory comprises a DDR-I SDRAM.

22. The random access memory of claim 18, wherein the memory comprises a DDR-II SDRAM.

23. A random access memory comprising:

means for receiving a first data strobe and generating a second data strobe from the first data strobe, wherein the second data strobe latches in first signals during a write operation; and

means for preventing the second data strobe from latching in second signals after latching in the first signals.

24. The random access memory of claim 23, wherein the means for preventing comprises:

means for indicating the first signals are latched, wherein the means for indicating provides an indication; and

means for locking the second data strobe to a logic level based on the indication.

25. The random access memory of claim 24, wherein the means for locking comprises:

means for latching a first output based on the first data strobe and the indication; and

means for latching a second output based on the first data strobe and the first output, wherein the means for latching a second output locks the second data strobe to the logic level.

26. A method for rejecting noise in a random access memory, comprising:
indicating that a burst of data signals are received;
setting a first flag based on the indication;
setting a second flag based on the first flag; and
locking a first data strobe signal to a logic level based on the second flag.

27. The method of claim 26, wherein indicating that a burst of data signals are received comprises counting clock cycles up to a set value.

28. The method of claim 27, wherein the burst length is one of 2, 4, 8, 16, and 32.

29. The method of claim 26, wherein indicating that a burst of data signals are received comprises shifting a shift register for each data signal in the burst of data signals up to a set value.

30. The method of claim 29, wherein the burst length is one of 2, 4, 8, 16, and 32.

31. The method of claim 26, wherein setting a first flag comprises:
receiving a second data strobe signal;
receiving the indication; and
latching in the first flag based on a state of the second data strobe signal.

32. The method of claim 26, wherein setting a second flag comprises:
receiving a second data strobe signal;
receiving the first flag; and
latching in the second flag based on a state of the second data strobe signal.